MBI5040 Application Note

Foreword

MBI5040 is an advanced 12-/16-bit PWM LED driver IC with 8-bit digital dot correction. Dot correction of each LED pixel can provide uniformed LED brightness and accurate LED color for high-end LED display panels. The traditional method to execute dot correction is through controllers. However, it is costly and complex. It will increase the loading of controllers and the limited control of LED pixels. The new digital dot correction designed in MBI5040 not only unifies the LED brightness and avoids the LED color wavelength shift during the dot correction process, but also reduces the loading and the cost of controllers.

MBI5040 provides constant output current from 2mA to 60mA for 16 output channels individually. It also provides in-message error detection, compulsory error detection, 7-bit current gain adjustment and thermal protection.

This article provides users application note when using MBI5040, such as grayscale data input method, power-on sequence, and configuration register setting for each function.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Power-on Sequence

Figure 1 shows the recommended power-on sequence. The power for MBI5040 (V_{DD}) should be turned on first, and then is the power of control board (V_{CC}). The control signals should be sent out after all the power of V_{DD} and V_{CC} are stable 3 to 5 seconds.

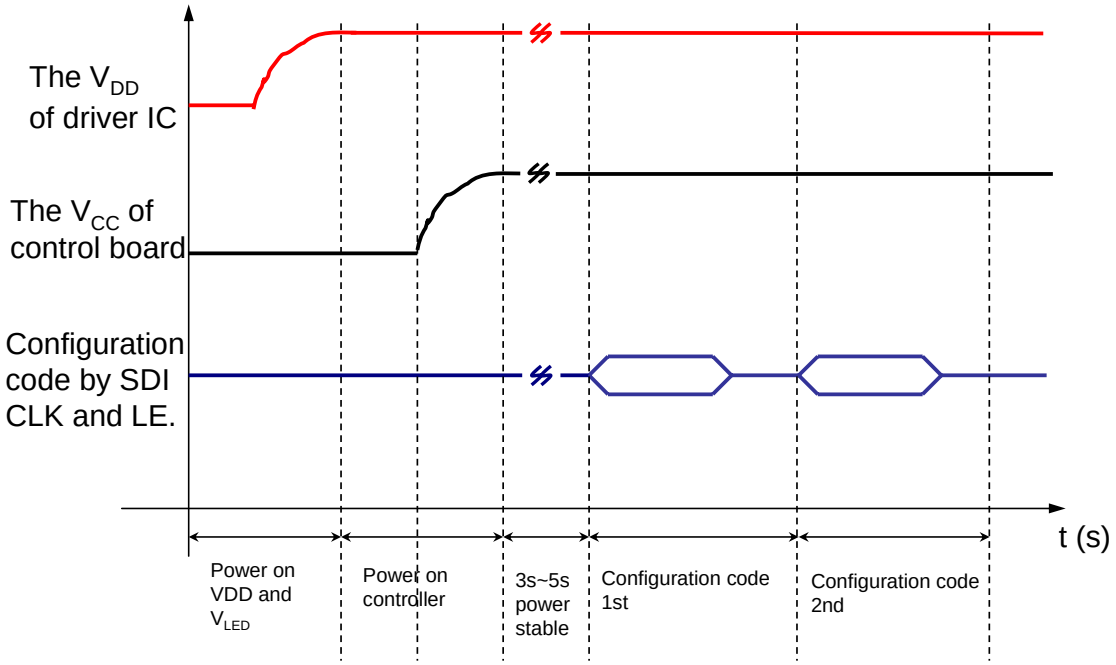

Figure 1. Power on sequence

IC Initial State

As the power of MBI5040 is turned on, the data in shift register is random due to non-reset action. Before the gray scale data sends into MBI5040, there is no PWM duty cycle in MBI5040 even the clock frequency of gray scale is running.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Grayscale data input

The shift register's length of 16-bit grayscale is 256 and the shift register's length of 12-bit grayscale is 192. The sequence to input the grayscale data for both 16-bit and 12-bit PWM of MBI5040 is from OUT15, OUT14, OUT13… to OUT0.

The method to input the grayscale data of N pieces MBI5040 in cascaded is to input the grayscale data of IC_N first, then the IC_{N-1}, till to the last, the IC_1. The data is latched by LE, which is containing the last 256 DCLKs for 16-bit PWM or the last 192 DCLKs for 12-bit PWM. Figure 2 shows the data sequence for MBI5040 16-bits PWM grayscale. The rising edge of DCLK is to trigger the SDI signal and the falling edge of DCLK is to multiply the data of grayscale and dot correction.

After the falling edge of DCLK, the LE should keep high 10ns at least.

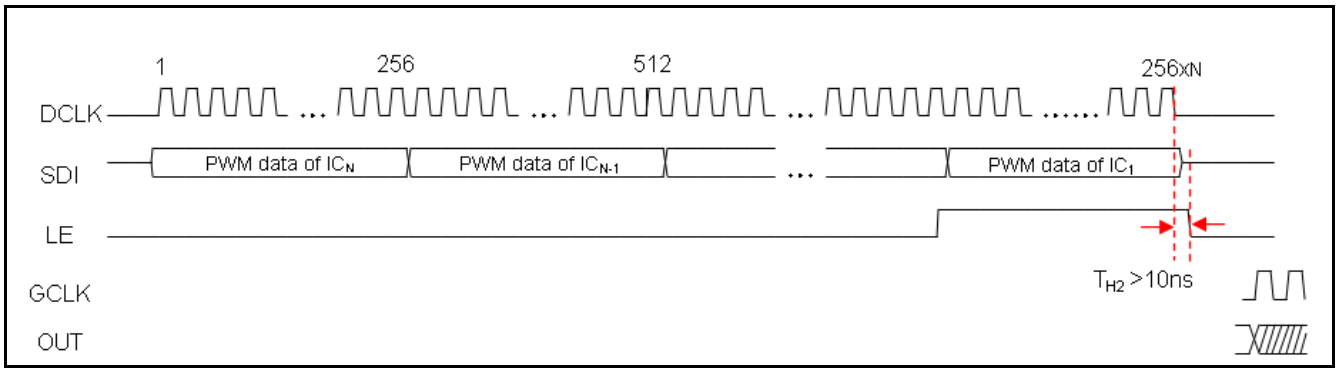

Figure 2. The data sequence for MBI5040 16-bits PWM grayscale.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

The differences between auto-synchronization mode and manual-synchronization mode

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Bit D of the configuration register is to select PWM data synchronization mode.
Auto-synchronization mode is suitable for static type LED display, and manual-synchronization mode is for time-multiplexing type LED display.
When the MBI5040 operates in auto-synchronization mode, the grayscale data, which is loaded by the control signal, will store in the internal buffer of MBI5040 till PWM counter renews the count period then update the data. The advantage of auto-synchronization mode is the signal control side does not need to care about the synchronization issue between display image and grayscale data update. In auto-synchronization mode, MBI5040 only needs a GCLK with fixed frequency and then MBI5040 can automatically update data in the correct timing. At the moment, the grayscale counter will not be interrupted by the next new grayscale data. Besides, the frequency of data refresh can not be higher than the frequency of one PWM cycle.
Table 1 lists the PWM count period of auto-synchronization and manual-synchronization modes. In auto-synchronization mode, the count period of 16-bits S-PWM is 1024, and 12-bits is 64. The count period of S-PWM is different from the conventional PWM.

Table 1. The count period of PWM data synchronization mode

Mode	Auto-synchronization		Manual-synchronization
Count period	S-PWM	Conventional PWM	S-PWM, Conventional PWM
16-bits	1024	65536	After grayscale data is latched.
12-bits	64	4096	After grayscale data is latched.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

The differences between continuous counting mode and one-shot mode

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Bit C of the configuration register is to select PWM counter mode, continuous counting or one-shot counting. Continuous counting mode is suitable for static type LED display, and one-shot counting mode is for time-multiplexing type LED display.

When the MBI5040 operates in continuous counting mode, it will continuously repeat the PWM cycle and turn on the output channels according to the image data until the next image data is correctly recognized, as figure 3 shows.

When the MBI5040 operates in one-shot counting mode, it will run the PWM cycle for each image data one time. If the next image data is not recognized yet, it is recommended to add a clock after GCLK has run a PWM cycle to stop the output channels. Take 16-bits PWM in manual synchronization for example, after the GCLK has counted 65536 clocks and then stops, some channels keep turned-on while the other channels keep turned-off, as figure 4 shows. If the GCLK counts 65536 and add extra one clock and then stops, all the channels are turned-off, as figure 5 shows.

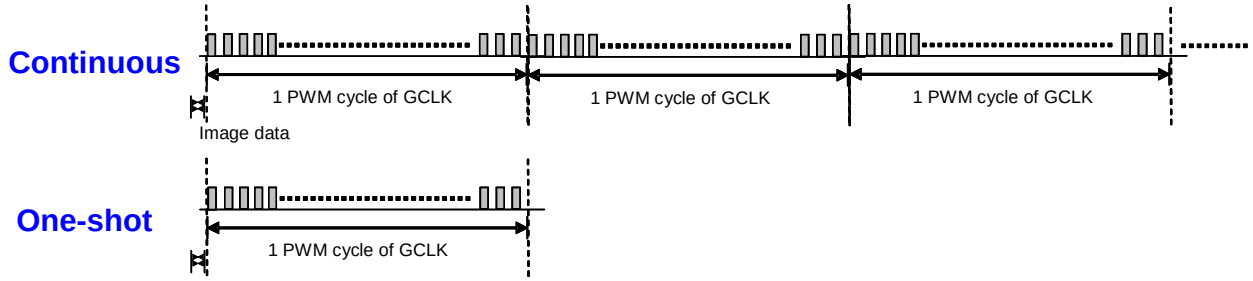

Figure 3. PWM counting modes

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

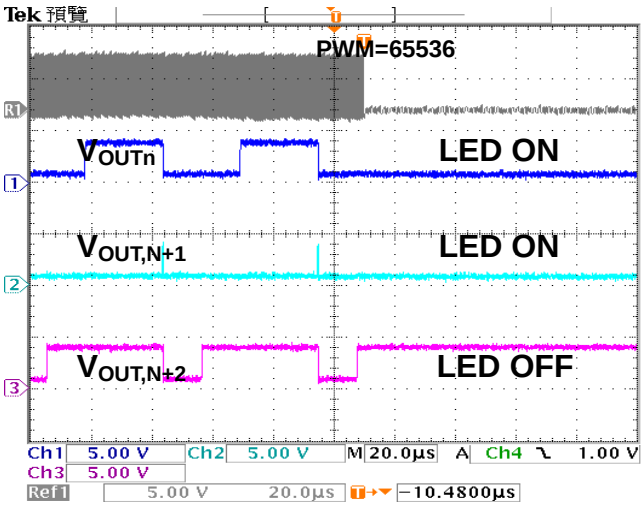

Figure 4. After PWM counts 65536, not all the output channels turn off. Run 16-bits PWM grayscales in one-shot mode, if PWM counts 65536, some channels keep turned-on while the other channels keep turned-off.

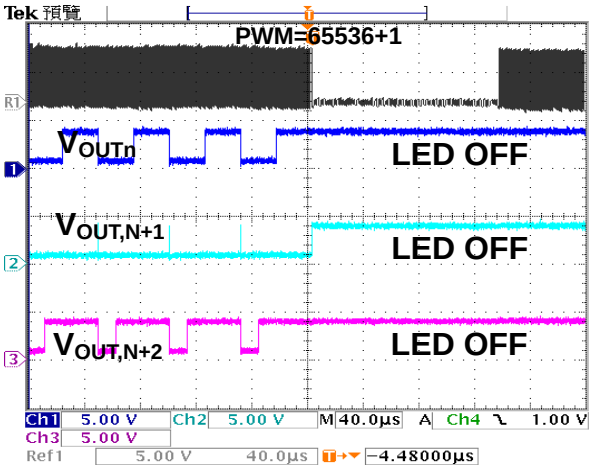

Figure 5. After PWM counts 65536+1, all the output channels turn off. Run 16-bits PWM grayscales in one-shot mode, If the GCLK counts 65536+1 and then stops, all the channels are turned-off.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Dot Correction

MBI5040 dot correction can compensate the variations in LED brightness. When the dot correction data inputs to IC, it will be memorized into the register of 8-bit dot correction till the V_{DD} of MBI5040 is turned off or the dot correction data is re-written. As the gray scale data inputs to IC, the product of gray scale data and dot correction data will output by PWM duty cycle. Because the LED display keeps PWM duty cycle, it can also avoid the LED color wavelength shift.

Dot Correction Setting Method

Each output channel of MBI5040 has 8-bit dot correction. The length of dot correction for 16 channels is 128-bit (8x16). MBI5040 can input the dot correction data when receiving one LE pulse containing one DCLK, and shift register's length of MBI5040 changes to 128-bit automatically. The data sequence of each IC is from OUT15, OUT14, OUT13.... to OUT0.

The method to leave the dot correction setting mode is by one LE pulse containing 0 DCLK. After that, shift register's length recovers to the length of PWM gray scale. Figure 6 is the circuit diagram of setting dot correction for one LED driver, and figure 7 is the circuit diagram of setting dot correction for N pieces LED driver.

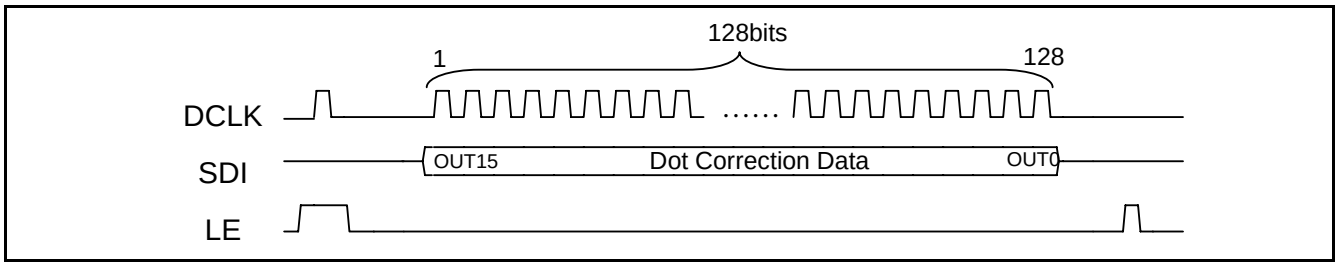

Figure 6. The circuit diagram of setting dot correction for one LED driver IC

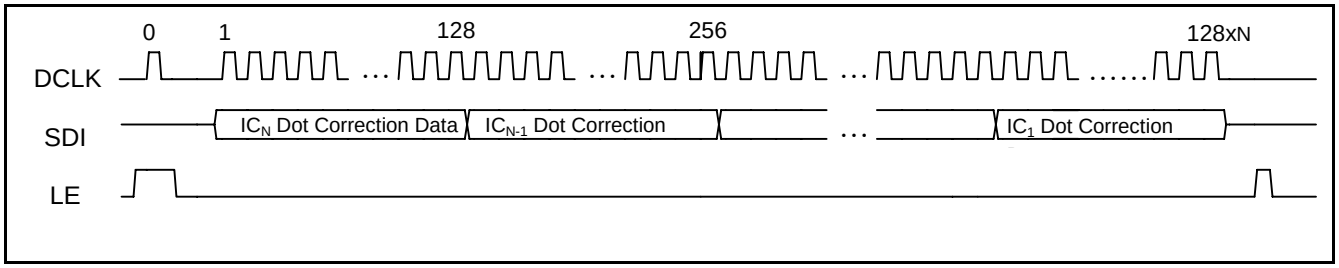

Figure 7. The circuit diagram of setting dot correction for N pieces LED driver ICs

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Dot Correction Compensation Formula

MBI5040 compensate the variations in LED brightness from the product of gray scale data and dot correction data. Following is the detailed computing method. The 1st step is to add 1 to 8-bit dot correction data. The 2nd step is to multiply the modified data with 16(or 12)-bit PWM gray scale data, and the bit of multiplied data is 24(or 20). The 3rd step is to count 16(or 12)-bit from MSB to be the compensated gray scale data.

The formula of 16-bit PWM shows in (1):

Output [15:0] = MSB {GS [15:0] x (DC [7:0] +1)} .....(1)

The formula of 16-bit PWM shows in (2):

Output [15:0] = MSB {GS [11:0] x (DC [7:0] +1)}.....(2)

Take two cases for example,

Ex1: Suppose the gray scale data is the binary 1010-1010-1010-1010 for 16-bit, and the dot correction data is the binary 1000-1000. After computing, the new PWM data is the binary 0101-1011-0101-0100. Following is the computational process,

```
                  10001000   = 0d136    (d:decimal)
                +         1
                = 10001001   = 0d137
x                 1010101010101010   = 0d43690
= 01011011010101001111 1010
(Get 0101101101010100)       = 0d23380
```

Ex2: Suppose the gray scale data is 1100-1100-1100 for 12-bit, and the dot correction data is 1110-1110. After computing, the new PWM image data is 1011-1111-0010. Following is the computational process,

```
                  11101110   = 0d238    (d:decimal)
                +         1
                = 11101111   = 0d239
x                 110011001100   = 0d3276
= 101111110010011 10100
(Get 101111110010)           = 0d3058
```

When computing the compensated data by using the binary, user maybe get the multiples data but the bit is not 24(or 20). This is because the highest bit is 0. Please do not miss it.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Write/Read Configuration Register

The configuration register of MBI5040 is 16-bits. After receiving one LE pulse containing 5 DCLKs, the configuration register code of cascading N pieces will be written in turn. The sum of total configuration register code is 16xN. The configuration code of each MBI5040 shifts into IC sequentially from the Nth MBI5040 to the 1st MBI5040. In finial, receiving one LE pulse containing 0 DCLK to latch and write the configuration register code, as figure 8 shows.

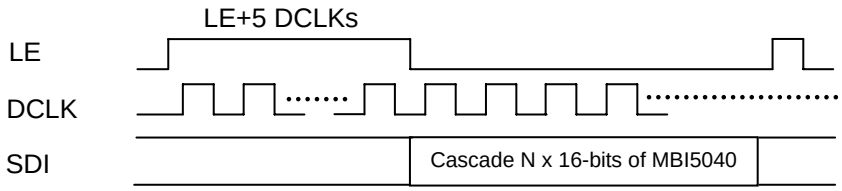

Figure 8. Write configuration register

To read the configuration register code, the first step is LE pulse should contain 5 DCLKs, and second is to receive one LE pulse containing 6 DCLKs. 16-bits configuration code of each MBI5040 will be shifted out sequentially from the Nth MBI5040 to the 1st MBI5040. In finial, to exit reading configuration register mode and recover the 16-bits configuration register to the length of PWM gray scale, MBI5040 should receive one LE pulse containing 3 DCLKs, as figure 9 shows.

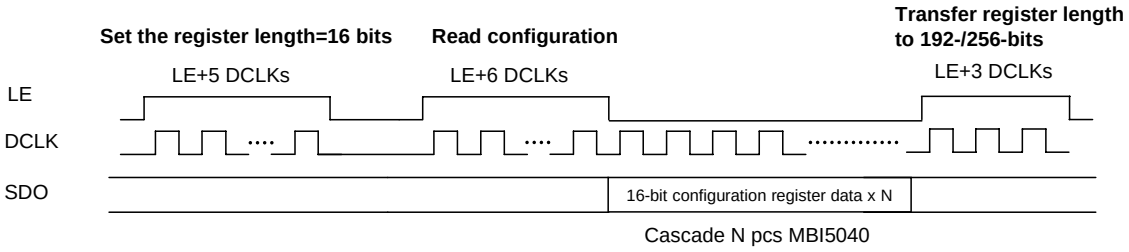

Figure 9. Read configuration register

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Frame rate and refresh rate

In display application, the number of frames, which is displayed in every second, is called the frame rate. The number of completed grayscales which are displayed in every second is called the refresh rate. The formula of refresh rate shows in (3).

$$\text{Refresh rate} = \frac{F_{GCLK}}{2^{\text{Grayscale bits}}} \qquad (3)$$

As the refresh rate gets higher, the repeated number of image data will also get higher. Take one example to explain it.

Assume the display board is 16-bits conventional PWM, controlled by static type. There are 96pcs of MBI5040 in cascaded. The frequencies of GCLK and DCLK are 30MHz, and the frame rate is 60Hz, then:

1. Refresh rate = $\frac{30\text{MHz}(F_{GCLK})}{2^{16}(\text{Grayscale})}$ = 457Hz, and it means there is 457 of completed grayscales can be displayed every second.

2. The repeated number of image data = Refresh rate ÷ Frame rate= $\frac{457(\text{Hz})}{60(\text{Hz})}$ =7.61

3. The consumption time of input grayscales data = $\frac{96(\text{ICs}) \times 16(\text{bits}) \times 16(\text{channel})}{30\text{M}(F_{DCLK})}$ = 0.82ms

It is recommended to set PWM counting as continuous counting by configuration register. Figure 10 shows the relationship between the frame rate and the refresh rate for the mentioned example.

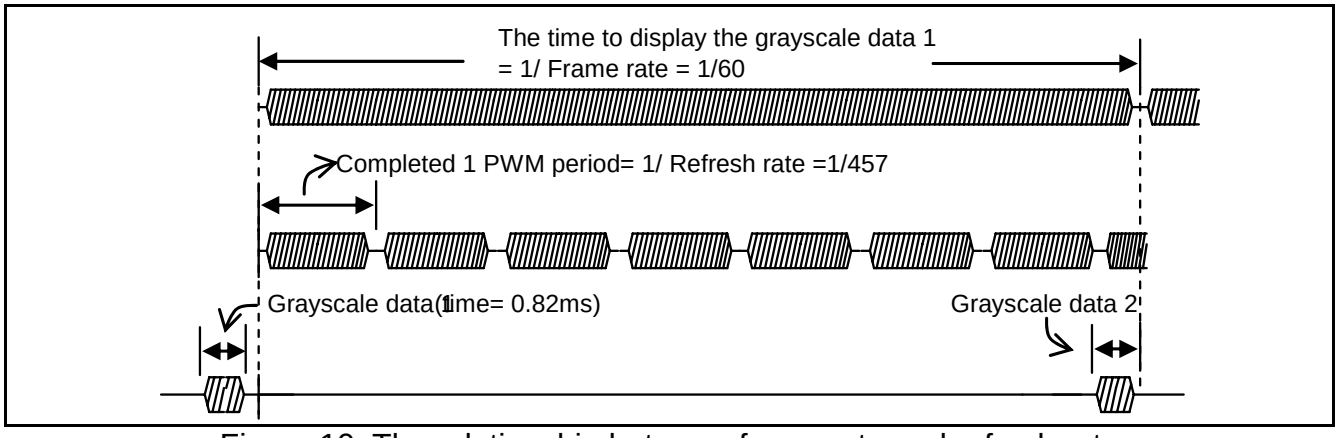

Figure 10. The relationship between frame rate and refresh rate

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

The S-PWM of MBI5040 can increases the visual refresh rate of static type LED application by 64x.

Assume the display board is 16-bits S-PWM, controlled by static type. There are 96pcs of MBI5040 in cascaded. The frequencies of GCLK and DCLK are 30MHz, and the frame rate is 60Hz, then:

1. Refresh rate = $\frac{30\text{MHz}(F_{GCLK})}{2^{16}(\text{Grayscale})}$ x 64 = 2930Hz. There is 2930 of completed grayscales can be displayed every second.

2. The repeated number of image data = Refresh rate ÷ Frame rate= $\frac{2930(\text{Hz})}{60(\text{Hz})}$ =48.8

3. The consumption time of input grayscales data = $\frac{96(\text{ICs}) \times 16(\text{bits}) \times 16(\text{channel})}{30\text{M}(F_{DCLK})}$ = 0.82ms

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

In-message Error Detection

If one of output channel of MBI5040 turns on for GCLKs at least, MBI5040 will execute the in-message error detection for this channel. The error messages include the open-/short-circuit error reports and thermal flag, and it will be put into the shift register after the gray scale data of the next frame is latched, as figure 11 shows.

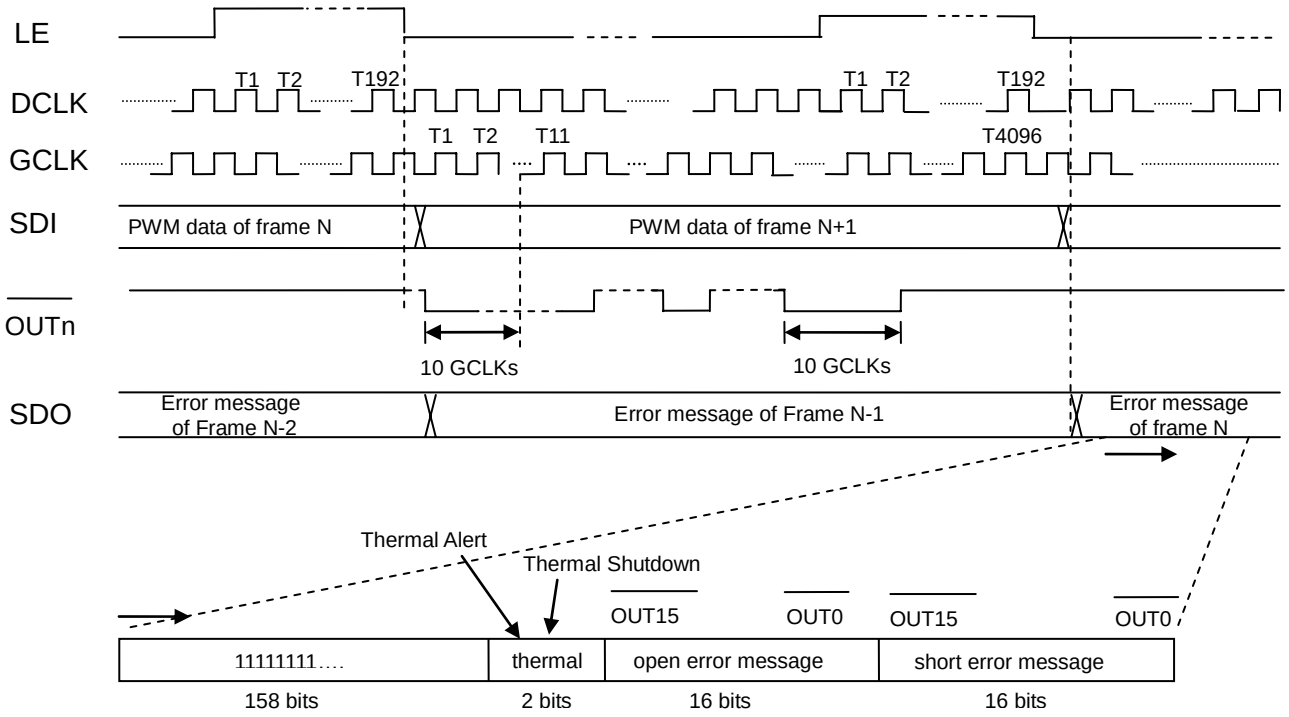

Figure 11. The timing sequence of compulsory error detection of 12-bit gray scale mode for 1 device

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Compulsory Error Detection

MBI5040 executes the compulsory error detection when receiving one LE pulse containing 4 DCLKs and stop it when receiving one LE pulse containing 0 DCLK. As the command (LE+0 DCLK) is implemented, the error message will be reported to shift register. When the next image data transfer into IC, the error message in shift register will be shifted out from SDO PIN. If display board has N devices of MBI5040 in cascaded, the length of error data will be Nx16-channelsx (16-/12-bits), and is the same as the length of image data. Figure 12 is the timing sequence of 12-bit gray scale mode's compulsory error detection. Figure 13 shows the error message shift-out status for N pieces of MBI5040 in cascaded.

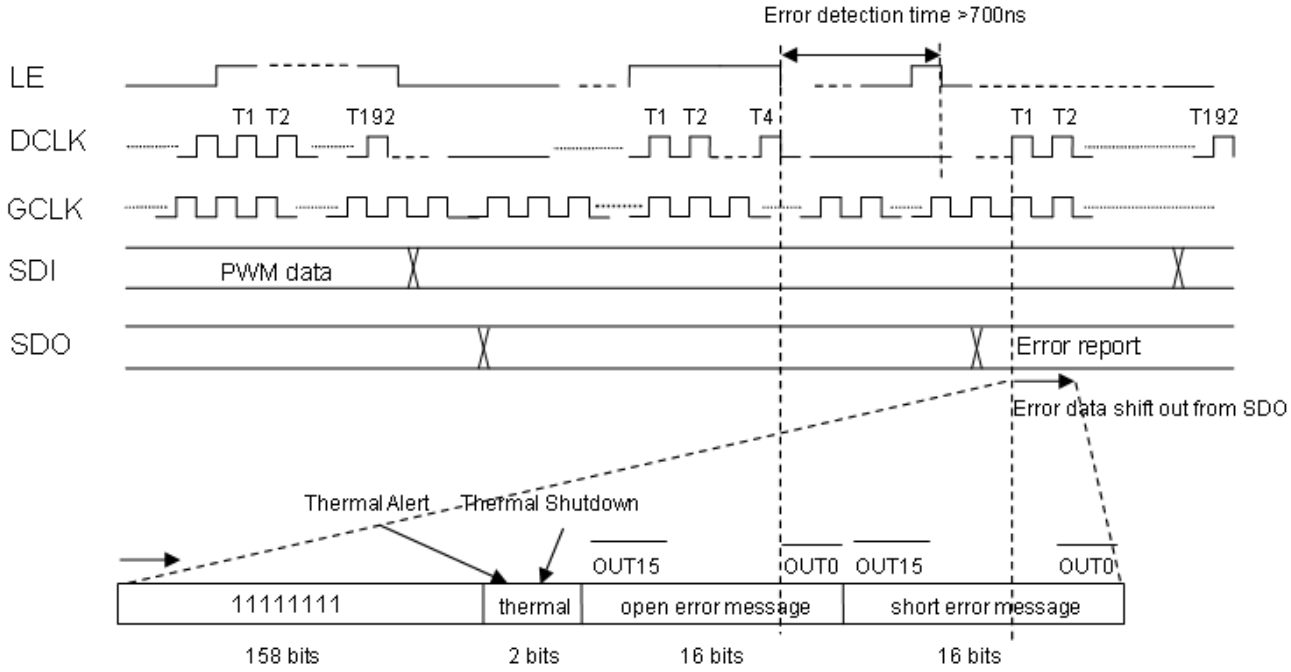

Figure 12. The timing sequence of 12-bit gray scale mode's compulsory error detection.

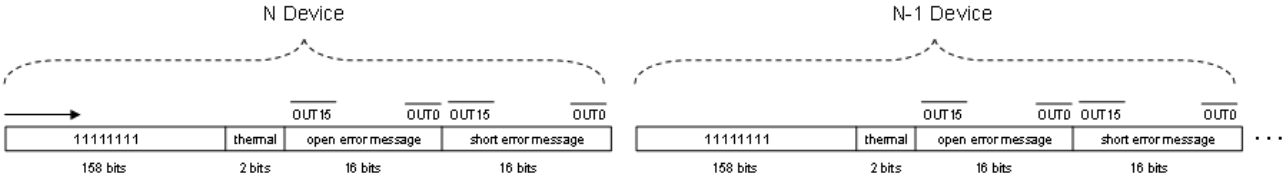

Figure 13. The error message shift-out status for N devices of MBI5040 in cascaded.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

Time-multiplexing Application

Here takes an example in 1/2 duty time-multiplexing application, the circuit is shown as figure 14, two rows of LEDs share an LED supply voltage, V_{LED}. By changing the MOSFET switching, the voltage of V_{LED} lights up two rows of LEDs in turn. Make sure the error detection and error message of first and second row of LEDs are separated.

During the error detection, the power of V_{LED} should keep stable. In addition, the supply voltage of previous LED row should be discharge to 0V completely before short circuit error detection is being processed. Connect resisters, R1 and R2, between V_{LED} and GND to discharge the remaining V_{LED}, as figure 14 shows. The purpose of capacitors, C1 and C2, who are located between Drain and Source of MOSFET, is to reduce the high voltage spike, which is caused by the parasitical effect.

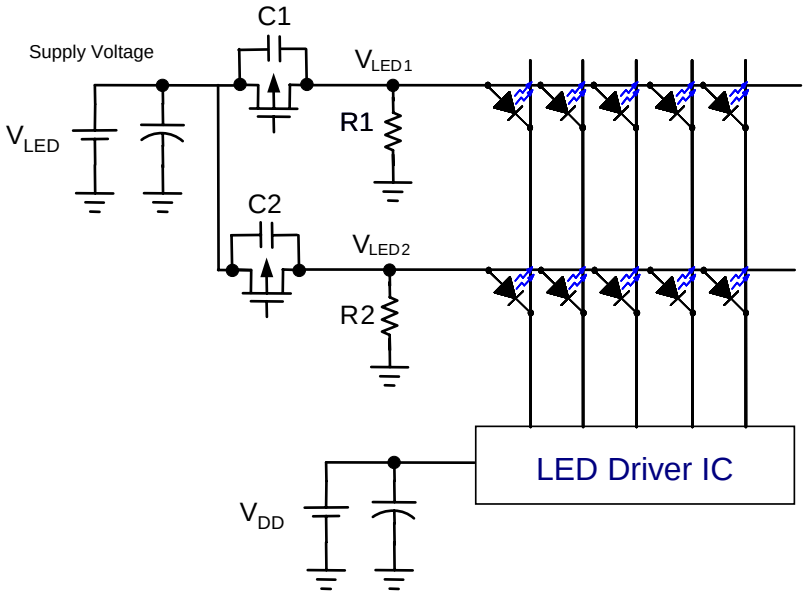

Figure 14. 1/2 duty Time multiplexing circuit.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw

The suggested timing diagram of compulsory error detection in time-multiplexing application is shown as figure 15. It is an illustration of the timing sequence of 12-bit gray scale mode.

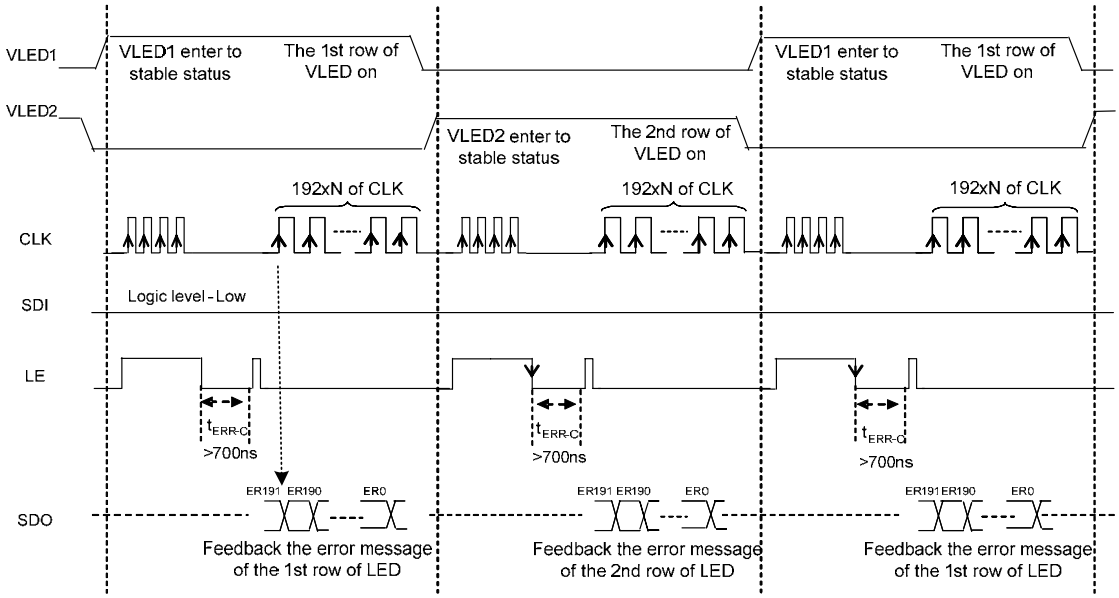

Figure 15. Compulsory error detection timing sequence in 1/2 duty time-multiplexing circuit

Conclusion

MBI5040 is an enhanced 12-/16-bit PWM LED display driver IC with 8-bit digital dot correction, in-message error detection, compulsory error detection, 7-bit current gain adjustment and thermal protection. User can follow this article to make sure MBI5040 works correctly.

Floor 6-4, No. 18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-0125, E-mail: info@mblock.com.tw